REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 4, 6-11, 13, 15-18, 21, 23-25, and 27-35 are pending in the present application. Claims 1, 4, 6, 7-11, 17, 18, 25, 27, 28, and 29 are amended, Claims 19, 20, and 26 are cancelled without prejudice, and Claims 32-35 are added by the present amendment.

In the outstanding Office Action, Claim 29 was rejected under 35 U.S.C. § 112, second paragraph; Claims 1, 4, 6-10, 17, 18, 20, 21, 23-29, and 31 were rejected under 35 U.S.C. § 101; and Claims 11, 13, 14, 15, 16, and 30 were indicated as allowable.

Applicants thank the Examiner for the indication of allowable subject matter and also for the courtesy of an interview extended to Applicants' representative on January 7, 2008. During the interview, clarifying claim amendments, similar to those presented herewith, were discussed for overcoming the § 101 rejection. The Examiner indicated that he would further review the amended claims in view of a filed response. Arguments presented during the interview are reiterated below.

Prior to discussing those arguments, Applicants note that an Information Disclosure Statement (IDS) is filed with this amendment and the IDS lists a technical report authored by one of the inventors of this application, i.e., Mr. T. Akenine-Möller. The document has been cited in the European Patent Office (EPO) in the counterpart of this application. The report has a date of April 23, 2002 on its front page and EPO has asserted that this is the publication date of this report. However, Applicants respectfully

submit that the date of April 23, 2002, is not the date when this report was made available to the public. As can be seen from the documents enclosed with this amendment, a letter has been filed in EPO stating that the listed report was not known to public or published before December 20, 2002, the date of the European patent application EP 1 431 920 A1 from which this application claims priority. The actual publication date of this report is June 2003, after the filing date of the European patent application EP 1 431 920 A1 from which this application claims priority. In support of these facts, please find enclosed three affidavits which are also being filed in EPO. In addition, the European patent application EP 1 431 920 A1 (in English) is filed herewith, to perfect the priority. Thus, it is believed that the enclosed report authored by one of the inventors is not prior art.

Regarding the rejection of Claim 29 under 35 U.S.C. § 112, second paragraph, this claim has been amended to more clearly indicate that the claim is directed to the method of Clam 11 and not to the pattern itself. No new matter has been added. Accordingly, it is respectfully requested this rejection be withdrawn.

Regarding the rejection of Claims 1, 4, 6-10, 17, 18, 20, 21, 23-29, and 31 under 35 U.S.C. § 101, the independent claims have been amended as discussed next.

Independent Claim 1 has been amended to recite a system for generating anti-aliased images as shown, for example, in Figure 1 and as disclosed in the specification, for example, at page 3, lines 31-32, and in the paragraph bridging pages 4 and 5. No new matter has been added. Dependent Claims 4, 6, 7-10, 27, and 28 have been amended to be consistent with amended Claim 1. Thus, it is respectfully submitted that

independent Claim 1 and each of the claims depending therefrom are directed to statutory subject matter.

Independent Claim 11 has been amended to more clearly recite steps of the method, as suggested by the Examiner during the interview. No new matter has been added. Accordingly, it is respectfully submitted that amended Claim 11 and each of the claims depending therefrom are directed to statutory subject matter.

Independent Claim 17 has been amended to more clearly recite a system for generating anti-aliased images, in a similar manner to Claim 1. The claim amendments find support in the specification, for example, in the same paragraphs discussed above with regard to independent Claim 1 and also in Figure 1. No new matter has been added. Accordingly, it is respectfully requested that amended Claim 17 is directed to statutory subject matter.

Independent Claim 18 has been amended to recite that a graphical processor is implemented in hardware as recited in Claim 19 and thus, dependent Claim 19 has been cancelled. In addition, Claim 20 has been cancelled and new independent Claim 32 has been added, to recite the features of independent Claim 18 and dependent Claim 20, but written to be directed to statutory subject matter. Further, new dependent Claims 33-35 have been added and are similar to Claims 21, 23, and 24, respectively. No new matter has been added. Accordingly, it is respectfully submitted that amended Claim 18, new independent Claim 32 and each of the claims depending therefrom are directed to statutory subject matter.

Independent Claim 25 has been amended to recite a computer-readable medium as suggested by the outstanding Office Action in the paragraph bridging pages 2, 3, and 4. No new matter has been added. Accordingly, it is respectfully submitted that amended Claim 25 and each of the claims depending therefrom are directed to statutory subject matter.

Thus, it is believed that all the outstanding rejections are overcome.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested. Should the Examiner have any questions regarding this response or the application in general, he is invited to contact the undersigned at (540) 361-2601.

Respectfully submitted,

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Affidavit

IN THE MATTER OF European Patent Application No. 02028537.5 to
TELEFONAKTIEBOLAGET LM ERICSSON (publ)

I, Tomas Akenine-Möller, Professor, Computer Science, Faculty of Engineering, Lund University, Sweden, hereby state as follows:

1) I am one of the inventors of the subject matter of European Patent Application 02028537.5, filed in the name of Telefonaktiebolaget LM Ericsson (publ) on 20 December 2002.

2) I am, and already was at the time of the invention of the subject matter of European Patent Application 02028537.5, well aware of absolute novelty being one requirement for patentability.

3) The first time I made any subject matter of European Patent Application 02028537.5 available to members of the public was in January 2003 when I submitted a paper to the organizers of the SIGGRAPH 2003 conference on computer graphics and interactive techniques. The paper included a description of a multisampling scheme, "FLIPQUAD", which is also described in European Patent Application 02028537.5. The actual conference took place on 27-31 July 2003 in San Diego, CA, USA.

4) I am the author of a technical report having the heading:

"FLIPQUAD: Low-Cost Multisampling Rasterization
Tomas Akenine-Möller
Chalmers University of Technology
Technical Report 02-04
23 April, 2002"

The date indicated in the heading of this technical report, i.e. 23 April, 2002, is the date when I finished writing the report.

5) I understand that the technical report referred to above in paragraph 4) has been cited by the Examining Division of the European Patent Office as alleged prior art document D3 against the pending claims of European Patent Application 02028537.5. I testify, however, that at the filing date of European Patent Application 02028537.5, i.e. 20 December 2002, I had not yet made this technical report available to the public.

6) Subsequently, well after the filing of European Patent Application 02028537.5, I published the technical report referred to above in paragraph 4) on my personal home page on a server operated by Department of Computer Science and Engineering, Chalmers University of Technology, Sweden. At the time, I held a part-time position as Assistant Professor at this Department. This publication on my personal home page occurred no earlier than in June of 2003, I believe, and in any event well after the filing date of European Patent Application 02028537.5.

7) In addition, well after the filing of European Patent Application 02028537.5, I also published the paper referred to above in paragraph 4) on my personal home page on a server operated by the Computer Science department, Faculty of Engineering, Lund University, Sweden. I joined this department as Associate Professor in March 2004. Therefore, I am certain that this publication on my personal home page took place no earlier than March 2004.

I MAKE THIS STATEMENT BELIEVING THE FACTS HEREIN TO BE TRUE

Tomas Akenine-Möller

LUND, 2008-03-25

(Place and date)

TO WHOM IT MAY CONCERN

Affidavit

IN THE MATTER OF European Patent Application No. 02028537.5 to TELEFONAKTIEBOLAGET LM ERICSSON (publ)

I, Ewa Cederheim-Wäingelin, hereby state as follows:

1) Since February 1996, I hold a position as Senior Secretary at the Department of Computer Science and Engineering, Chalmers University of Technology, Sweden.

2) I understand that a technical report bearing the heading:

"FLIPQUAD: Low-Cost Multisampling Rasterization
Tomas Akenine-Möller
Chalmers University of Technology
Technical Report 02-04
23 April, 2002"

has been the subject of discussions during patent examination proceedings before the European Patent Office.

3) The author of the paper referred to above under paragraph 2), i.e. Tomas Akenine-Möller, was employed as Assistant Professor by the Department of Computer Science and Engineering, Chalmers University of Technology, Sweden, between 2001 and 2004.

4) Being an employee, Tomas Akenine-Möller had a personal home page allocated to him on a server operated by the Department of Computer Science and Engineering, Chalmers University of Technology, Sweden. Publication of information on the personal home page was controlled by Tomas Akenine-Möller himself.

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5) I am not aware of any publication of the technical report referred to above in paragraph 2) on any web pages belonging to the Department of Computer Science and Engineering at Chalmers University of Technology, except possibly on the personal home page referred to above in paragraph 4).

I MAKE THIS STATEMENT BELIEVING THE FACTS HEREIN TO BE TRUE

Ewa Cederheim-Wäingelin

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Göteborg, March 26, 2008
(Place and date)

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Affidavit

IN THE MATTER OF European Patent Application No. 02028537.5 to
TELEFONAKTIEBOLAGET LM ERICSSON (publ)

I, Lars Nilsson, hereby state as follows:

1) Since 15th of May 2002 I hold a position as Systems Manager, Computer Science, Faculty of Engineering, Lund University, Sweden.

2) I understand that a technical report bearing the heading:

"FLIPQUAD: Low-Cost Multisampling Rasterization
Tomas Akenine-Möller
Chalmers University of Technology
Technical Report 02-04
23 April, 2002"

has been the subject of discussions during patent examination proceedings before the European Patent Office.

3) The author of the technical report referred to above under paragraph 2), i.e. Tomas Akenine-Möller, has held a position as Associate Professor, subsequently Professor, at the department of Computer Science, Faculty of Engineering, Lund University, Sweden, since March 2004.

4) Being an employee, Tomas Akenine-Möller has a personal home page allocated to him on a server operated by the department of Computer Science, Faculty of Engineering, Lund University, Sweden. The address to this personal home page is http://www.cs.lth.se/home/Tomas_Akenine_Moller/. Publication of information on the personal home page is controlled by Tomas Akenine-Möller himself.

5) In the years 2002-2003, Tomas Akenine-Möller was not employed by the department of Computer Science, Faculty of Engineering, Lund University, Sweden.

Consequently, there was no personal home page allocated to him at the department of Computer Science, Faculty of Engineering, Lund University, Sweden, during the years 2002-2003, and it would have been technically impossible for him to publish any information on such a personal home page during those years.

I MAKE THIS STATEMENT BELIEVING THE FACTS HEREIN TO BE TRUE

Lars Nilsson

Lund, 8nd of April 2008

(Place and date)

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(54) Low-cost supersampling rasterization

(57) A sampling pattern covering an array of pixels for use in an anti-aliasing system is disclosed where each pixel has a pattern of sample points at the edges of the pixel. Moreover is the sample point pattern of each pixel a mirror image and different from the pattern of a directly neighboring pixel.

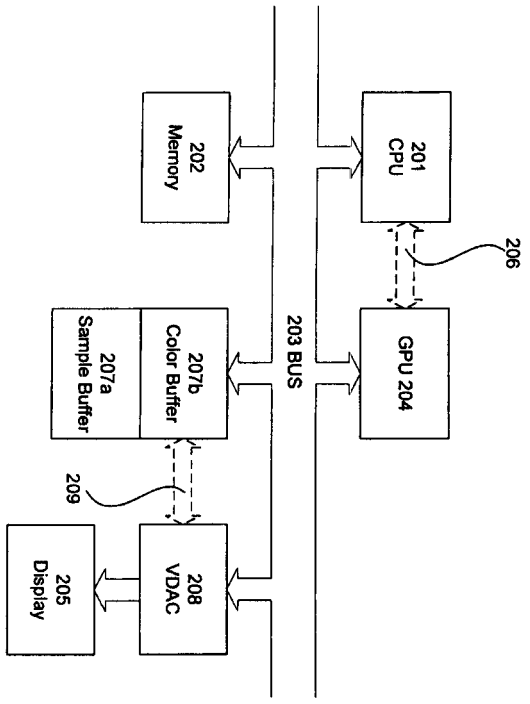

Fig 1

EP 1 431 920 A1

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Description

Technical Field

[0001] Generally, the present invention relates to graphic processing and more specifically to a method and apparatus for producing high-quality anti-aliased graphic pictures at high frame rates with low computational cost.

Description of the Prior Art

[0002] Since the early days of computer graphics, aliasing has been a problem when presenting still or moving pictures on a display.

[0003] One approach to combat the low visual quality of aliased pictures is to use what is known as supersampling. Supersampling will provide a good picture quality but has the drawback of a low frame rate due to a heavy computational burden. More specifically, supersampling renders a picture at a higher resolution than the final resolution that is displayed on the screen. This is done by rendering multiple sub-pixel samples for each pixel to be displayed, i.e. the value of each pixel will be a weighted sum of the sub-pixel sample values. For example may each displayed pixel comprise the filtered, weighted sum of a group of four sub-pixel samples inside a pixel. As can be readily understood, this implies that the graphics hardware has to process four times as many samples for each displayed pixel.

[0004] The patent document WO-00/33256 discloses a system that utilizes a supersampling scheme. Each pixel is divided into a more or less fine-meshed grid which defines a sub-pixel grid, where sample points may be located. The sub-pixel sample points may be arranged in many different configurations inside the pixel boundaries. The sample point configuration pattern is then repeated for every pixel to be rendered. The final value for each pixel comprises the weighted sum of three or more samples located in sub-pixels according to the discussion above.

[0005] The patent document US-6,057,855 discloses a system for determining a value for an anti-aliased pixel. In similarity to the above document, the system uses a supersampling scheme for determining the sample values at multiple sub-pixel sample locations.

[0006] In order to lower the computational burden for producing anti-aliased pixels, a modified supersampling scheme may be used. The key idea of this supersampling scheme is to place the sub-pixel sample locations in such positions so that the value of one or more of the sample locations may be used for calculating the final value for more than one pixel. A supersampling scheme of this kind is also referred to as a sample-sharing scheme.

[0007] The GeForce3 graphics processing unit from NVIDIA Corporation, Santa Clara, USA provides hardware that supports supersampling and sharing of sub samples between pixels. The supersampling scheme is referred to as "Quincunx" and presents a sub-pixel sample pattern in form of a "5" on a die, i.e. five sub-pixel samples are used for calculating the value of the final pixel. However, due to the placing of the sample locations, only two samples per pixel need to be calculated; the rest of the sample values are obtained from the neighboring pixels. The center sub-pixel sample is given the weight 0.5 while the peripheral sub-pixel samples are given the weight 0.125 each. In a subsequent step, the sub-pixel samples are filtered in the same way as with an ordinary supersampling scheme.

[0008] Detailed information regarding the Quincunx scheme is found in "Technical Brief, HRAA: High-Resolution Antialiasing through Multisampling" from NVIDIA Corporation. This document is e.g. retrievable from the NVIDIA Corporation web site "www.nvidia.com".

[0009] The number of gray levels between black and white (in a monochrome scheme) depends on how many sub-pixel sample points that are used. In case four sub-pixel sample locations are used, there will at best be three gray shades between black and white. Consequently, the Quincunx scheme above will at best provide four shades of gray. However, as will be discussed below, the effective number of gray shades for the Quincunx scheme may be as low as two.

[0010] Accordingly, the computational burden for producing anti-aliased pixels is a problem in modern computer graphics systems. As is easily understood, the problem becomes even bigger if an anti-aliasing scheme is to be used for producing moving pictures on a device with reduced computational capability, such as a mobile telephone or a PDA (personal digital assistant).

Summary of the Invention

[0011] The present invention seeks to provide a method and apparatus for producing high-quality anti-aliased pictures at a low computational cost.

[0012] This object has been achieved by a sampling pattern covering an array of pixels, where each pixel has a pattern of sample points at the edges of the pixel, and where the sample point pattern of each pixel is a mirror image and different from the pattern of a directly neighboring pixel.

Brief Description of the Drawings

[0013] A preferred embodiment of the present invention will now be described with reference to the accompanying drawings, in which:

FIG. 1 is a schematic block diagram illustrating a graphics system for creating anti-aliased pictures,

FIG. 2 is a schematic drawing illustrating the calculation of the sub-pixel sample locations according to the present invention,

FIG. 3 is a schematic illustration of a mirroring step

according to a preferred embodiment of the present invention,

FIG. 4 is another schematic illustration of a mirroring step according to a preferred embodiment of the present invention

FIG. 5 is a schematic flow chart illustrating the method for producing anti-aliased pictures according to the present invention, and

FIG. 6 is a schematic drawing illustrating the calculation of pixel values according to the present invention compared to a prior art scheme.

FIG 7 is a graphic comparison between no anti-aliasing, a prior art scheme and the anti-aliasing scheme according to the present invention.

Detailed Disclosure of a Preferred Embodiment

[0014] Figure 1 is a block diagram of an example of a system for drawing lines or polygons. A CPU (Central Processing Unit) 201 is connected to a memory 202 by means of a data bus 203. The memory 202 comprises the application program that is run on the system, e.g. a computer game or a CAD (Computer Aided Design) program. As with most computer systems, the CPU 201 fetches instructions in the memory 202 and executes them in order to perform specific tasks. In this context, a task for the CPU 201 is to provide a GPU 204 (Graphics Processing Unit) with information regarding the objects that shall be drawn on a display 205. It is emphasized that the GPU 204 may be in form of a processor, such as a DSP (Digital Signal Processor), or in form of an ASIC (Application Specific Integrated Circuit), FGPA (Field-Programmable Gate Array), hard-wired logic etc, or it may be executed on the CPU 201. The GPU 204 is also connected to the bus 203 but may as well be connected to the processor by means of a separate high-speed bus 206 in case a lot of information is to be transferred between the CPU 201 and the GPU 204. The data transfers on the separate high-speed bus 206 will then not interfere with the data traffic on the ordinary bus 203.

[0015] Moreover, a display memory 207 is also connected to the bus 203 and stores information sent from the GPU 204 regarding the pictures (frames) that shall be drawn on the display 205. More specifically, the display memory contains a sample buffer 207a and a color buffer 207b. As will be discussed below, according to the present invention, the sample buffer 207a contains approximately twice as many samples as there are pixels in the final color buffer 207b. The color buffer 207b holds the colors of the pixels to be displayed on screen after the rendering of an image is complete. As with the interconnection between the CPU 201 and the GPU 204, the display memory 207 may be connected directly to the GPU 204 by means of a separate, high-speed bus. Since the GPU 204 and the display memory 207 normally are used for producing moving images, it is preferred that the link between these two units is as fast as possible and does not block the normal traffic on the bus 203.

[0016] The display memory 207 is connected to a VDAC 208 (Video Digital to Analog Converter), either by means of the shared bus 203 or by a separate high-speed bus 209, which reads the information from the color buffer 207b and converts it to an analog signal, e. g. a RGB (Red, Green, Blue) composite signal, that is provided to the display 205 in order to draw the individual pixels on the screen.

[0017] As discussed above, many different techniques have been used in order to produce anti-aliased representations of lines and polygons. As can be seen in figure 2a and 2b, the present invention uses a variant of a super-sampling scheme. As with the Quincunx scheme, the sub-pixel sample locations 303-306 are placed at the edges of the pixel 301, 302. As discussed above, this allows for sample sharing between different pixels 301, 302 in the display memory 207.

[0018] However, the samples are not placed in the corners of the pixel 301, 302 as with the Quincunx scheme. Instead, in a preferred embodiment, one sub-pixel sample location is defined for each edge of the pixel 301, 302 in a rotated square-shaped configuration and is given a weight of 0.25 each. This is explained in figure 2a and 2b by superimposing a grid over the pixel 301, 302 and defining a possible sample point wherever the grid intersects an edge of a pixel 301, 302. The equations for determining the precise sub-pixel sample locations are shown under figures 2a and 2b respectively. Alternatively, the edges of the pixels in the discussion above may be substituted by one or more mirroring planes in case the sampling pattern is translated in any direction. The mirror planes will then normally be parallel with the edges of the pixels and with spacing equal to the distance between the edges of the pixels. For example, the sampling pattern may be translated a small amount to the left, wherein the sub-pixel sample locations no longer resides on the edges of the pixels. In this case it is still possible to define one or more mirroring planes for creating a sample pattern according to the present invention. This will become apparent by the discussion below in relation to figure 3.

[0019] The placing of the sample locations 303-310 will break the symmetry of the configuration which will increase the anti-aliasing effect of near to vertical lines and near to horizontal lines. To illustrate this, lets assume a near to horizontal edge of a polygon that is drawn on a display across one or more pixels 301, 302. If e.g. the Quincunx scheme is used for producing an anti-aliased representation of the line, four sample points, one in each corner of the pixel 301, 302, will be used. For some pixels 301, 302, the edge will cover only the top part but will still cover the two uppermost sub-pixel sample locations. Consequently, by examining the values from the sub-pixel sample locations in the pixel 301, 302, the anti-aliased value of the pixel will be 0.25 even if half the pixel is covered by the edge (i.e. until the live covers the sub-pixel sample in the center). The pixel

will hence be incorrectly presented on the screen.

[0020] If the same situation applies with the use of the present invention a near to horizontal line, covering a small part of the top of the pixel 301, 302, will not cover both sub-pixel sample locations but only the sample location on the uppermost horizontal edge of the pixel 301, 302 due to the placing of the sample locations. The reason for mirroring the sample locations for every other pixel will be discussed below.

[0021] Figure 3 illustrates an important feature of the present invention. In accordance with the above, the sub-pixel sample locations 403-406 of the leftmost pixel 401 are not placed in the corners of the pixel as is the case with the Quincunx scheme. In the following text, this sub-pixel sample configuration will be referred to as "quad A". Correspondingly, a pixel 402 presenting a sub-pixel sample configuration that is a mirror image of "quad A" will be referred to as "quad B". As can be seen in figure 3, the sub-pixel sample locations 406-409 in the rightmost pixel 402 corresponds to the quad B locations according to the above. As mentioned above, by examining the configurations of quad A and quad B side-by-side it is evident that the sub-pixel sample locations 406-409 of quad B is a mirror image of the corresponding locations 403-406 in quad A reflected at the right vertical edge 410 of quad A (and consequently the left vertical edge of quad B).

[0022] By mirroring the locations of the sub-pixel sample locations 403-409 it is possible to share the sample 406 between the two pixels and still break up the symmetry of the configuration and achieve a better anti-aliasing result according to the above. Another important feature is that there is only one sample per row and column. In e.g. Quincunx, there are two samples for the top row.

[0023] Figure 4 further illustrates the anti-aliasing scheme according to the present invention. The upper left pixel 501 contains four sub-pixel sample points 510-513 in a quad A configuration. The pixel 502 to the right of this pixel 501 also contains four sub-pixel sample locations 513-516 in a quad B configuration, which are reflected at the right edge of the leftmost pixel 501. Moreover, a third pixel 503 also contains four sub-pixel sample points 516-519 in a quad A configuration. As can be seen from figure 4, the upper row of pixels 501-503 share one sub-pixel sample location 513, 516 between each pair of pixels 501-502, 502-503.

[0024] Next row starts with a pixel 504 presenting a quad B configuration of sub-pixel sample points 511, 520-522. The sample location 511 is shared between this pixel 504 and the pixel 501 on the row above. By examining the configurations of quad A (the topmost pixel 501) and quad B (the lower pixel 504) side-by-side it is evident that the sub-pixel sample locations 511,520-522 of quad B is a mirror image of the corresponding locations 510-513 in quad A reflected at the bottom horizontal edge 530 of pixel 501 (and consequently the top horizontal edge of pixel 504).

[0025] The next pixel 505 on the second row contains four sub-pixel sample points 515, 522-524 in a quad A configuration. What is important to notice is that this pixel 505 share one sample point 515 with the pixel 502 on the row above and one sample point 522 with the pixel 504 to the left. The same applies to the rightmost pixel 506 on the second row, which also shares two sample points 517, 524 with the neighboring pixels 503, 505.

[0026] Consequently, by using the mirroring scheme of the present invention, all pixels, except for the uppermost and leftmost pixels 501-504 on a display 205, require a calculation of only two new sub-pixel sample location values when determining the final value of the pixels 501-506. Alternatively, all pixels except the rightmost column and the bottommost row require only two samples.

[0027] The sample locations in the pixels may be traversed by scanning the lines from left to right. Alternatively, the scanning direction may be altered every other line in order to render the memory usage more effective. It is understood that any traversal scheme can be implemented in conjunction with the supersampling scheme according to the present invention.

[0028] Figure 5a is a flow chart illustrating a method for producing high-quality anti-aliased pictures according to a preferred embodiment of the present invention. In step 610 the CPU runs the application program (e.g. a computer game) and generates the 3D objects (normally polygons in form of triangles) that shall be converted into a 2D-presentation on the display.

[0029] Next, in step 620, the CPU or the GPU/hardware calculates the different visual effects that affect the appearance of the object on the display, such as lighting, clipping, transformations, projections, etc. As triangles are normally used when creating 3-D objects in computer graphics, the pixel coordinates of the vertices of the triangles are finally calculated.

[0030] In step 630 the CPU or the GPU/hardware interpolates texture coordinates over the polygon in order to ensure that a correct projection is obtained. In addition to this the CPU or GPU/hardware may also interpolate one or more colors, another set of texture coordinates, fog, and more. It also performs Z-buffer tests, and ensures that the final pixel obtains the correct color.

[0031] Figure 5b is a more detailed flow chart illustrating step 630 in figure 5a. To increase the intelligibility of the flow chart in figure 5b, references are also made to figure 6a. Step 631 is a polygon (triangle) setup stage where the CPU or the GPU/hardware calculates interpolation data that is used over the entire polygon 801.

[0032] A scan conversion is performed in step 632, wherein the CPU or the GPU/hardware identifies pixels 703 or sample points 704 that lie inside the boundaries 705 of the polygon 701. There are many different ways to perform this identification. A simple approach is to scan the horizontal rows one by one.

[0033] All visible sample points 704 are transferred to step 633 which calculates the color of each visible pixel

701 by means of the textures and the interpolated color (s). The color of each sample is written to the sample buffer 207a. After all polygons have been processed, the sample buffer 207a will contain the picture in a high-resolution format (2 samples pixel of the final image). Only visible samples are processed in this stage. Samples that are not visible, i.e. samples that are behind a previously drawn polygon, will not contribute to the final picture. In a final stage, the samples are filtered to produce a picture of correct size. More specifically, four samples per pixel will be averaged to form the final pixel color stored in the color buffer 207b.

[0034] With reference to figures 6a and 6b, a comparison will now be made between the Quincunx scheme and the scheme according to the present invention. The sub-pixel sampling pattern according to the present invention is illustrated in figure 6a, and the sub-pixel sampling pattern according to the Quincunx scheme is illustrated in figure 6b.

[0035] Assume that the inside of a triangle is colored white (encoded as 1.0), and the outside colored black (encoded as 0.0). Anything in between 0.0 and 1.0 represents a gray scale. Also, it should be noted that the same applies as well to colors or any other representation. As can be seen from the figures of this example, a polygon, in this case a triangle, is covering a 6 x 6 pixel matrix. However, the number of pixels are not restricted to this number and depends on the specific application, i.e. a desktop computer system will use a higher resolution (more pixels) than e.g. a mobile telephone. The same working principle applies to any system irrespective of the resolution of the system. In both figure 6a and 6b, pixels that are completely inside the triangle will obtain the value 1 (completely white). In the Quincunx scheme, this arises from the summing-up of the corner samples (each with the weight 0.125) and the center sample (with weight 0.5). Correspondingly, in the scheme according to the present invention, the same value arises from the summing-up of the four edge sampling positions (each with the weight 0.25).

[0036] In figure 6a, the leftmost column will obtain the values (from top to bottom): 0.25, 0.5, 0.5, 0.5, 0.5, and 0.25, where each number represents a gray scale color. That is, the vertices of the triangle will have a slightly darker shade of gray than the central part of the left edge of the triangle.

[0037] Correspondingly, in figure 6b, the leftmost column will obtain the values: 0.125, 0.75, 0.75, 0,25, 0.25, and 0.125. What is important is the abrupt jump between the third and fourth pixel in the column. As mentioned above, the calculated pixel values for a near to vertical line will always make an abrupt jump from 0.25 to 0.75 when the Quincunx scheme is used, even though it is theoretically possible to obtain a value of 0.375, 0.5, and 0.625. On the other hand, the mirroring scheme according to the present invention will give a smoother transition between the different possible pixel values.

[0038] Aliasing is very noticeable when drawing almost vertical lines and almost horizontal lines, and thus it is important that the anti-aliasing scheme produces good result when edges are near to vertical or near to horizontal.

[0039] The above reasoning is further illustrated in figures 7a-c, where a comparison between no anti-aliasing 7a, the Quincunx scheme 7b, and the scheme according to the present invention 7c is shown. The figures clearly illustrates that the anti-aliasing effect for both for a near to vertical as well as for a diagonal line is enhanced by the scheme according to the present invention. More specifically, the effective number of gray levels presented by the Quincunx scheme is reduced to two as described above while the scheme according to the present invention presents three levels of gray between black and white.

[0040] The present invention has been described above with reference to a preferred embodiment. However, other embodiments than the one disclosed herein are possible within the scope of the invention, as defined by the appended independent claims.

Claims

1. A sampling pattern covering an array of pixels for use in an anti-aliasing system, where each pixel has a pattern of sample points at one or more than one mirror plane within the array of pixels, **characterized in that**

   the sample point pattern of each pixel is a mirror image and different from the pattern of a directly neighboring pixel.

2. The sampling pattern according to claim 1, wherein the mirror planes are located on the edges of the pixel.

3. The sampling pattern according to claim 1 or 2, wherein the pattern has one sample point per pixel mirror plane.

4. The sampling pattern according to claim 1 to 3, wherein the (x, y) coordinates of the sample points for a pixel are related according to (0, a), (a, 1), (b, 0), and (1, b).

5. The sampling pattern according to claim 1 to 3, wherein the (x, y) coordinates of the sample points for a pixel are related according to (0, b), (a, 0), (b, 1), and (1, a).

6. The sampling pattern according to claims 4 or 5, wherein the sum "a+b" is in the range 0,5 - 1,5.

7. The sampling pattern according to claims 4-6, wherein a = 1/3 and b = 2/3.

8. The use of a sampling pattern according to any of claims 1-7 in a pixel anti-aliasing system.

9. The use of a sampling pattern according to claim 8 for processing a still image.

10. The use of a sampling pattern according to claim 8 for processing a video sequence.

11. A method for creating a sampling pattern covering an array of pixels for use in an anti-aliasing system, where each pixel has a pattern of sample points at the edges of the pixel, **characterized by**

defining the sample point pattern of each pixel so that it is a mirror image and different from the pattern of a directly neighboring pixel

12. The method according to claim 11, wherein the pattern has one sample point per pixel edge

13. The method according to claim 11 or 12, wherein the (x, y) coordinates of the sample points for a pixel are related according to (0, a), (a, 1), (b, 0), and (1, b).

14. The method according to claim 11 or 12, wherein the (x, y) coordinates of the sample points for a pixel are related according to (0, b), (a, 0), (b, 1), and (1, a).

15. The method according to claims 13 or 14, wherein the sum "a+b" is in the range 0,5 - 1,5.

16. The method according to claims 13 to 15, wherein a = 1/3 and b = 2/3.

17. An anti aliased image created by processing an image according to any of the steps 11-16

18. An anti-aliasing system comprising a GPU, wherein the GPU is adapted to define a pattern of sample points at the edges of a pixel, **characterized in that**

the GPU is adapted to define the sample point pattern of each pixel so that it is a mirror image and different from the pattern of a directly neighboring pixel

19. The system according to claim 18, wherein the GPU is implemented in hardware.

20. The system according to claim 18, wherein the GPU is implemented in software.

21. The system according to claims 18 to 20, wherein the (x, y) coordinates of the sample points for a pixel are related according to (0, a), (a, 1), (b, 0), and (1, b).

22. The system according to claims 18 to 20, wherein the (x, y) coordinates of the sample points for a pixel are related according to (0, b), (a, 0), (b, 1), and (1, a).

23. The system according to claims 21 or 22, wherein the sum "a+b" is in the range 0,5 - 1,5.

24. The system according to claims 21 to 23, wherein a = 1/3 and b = 2/3.

25. A computer program product directly loadable into an internal memory associated with a CPU, said CPU being operatively coupled to a GPU for defining a pattern of sample points at the edges of a pixel, comprising program code for

defining the sample point pattern of each pixel so that it is a mirror image and different from the pattern of a directly neighboring pixel

26. A computer program product as defined in claim 22, embodied on a computer-readable medium.

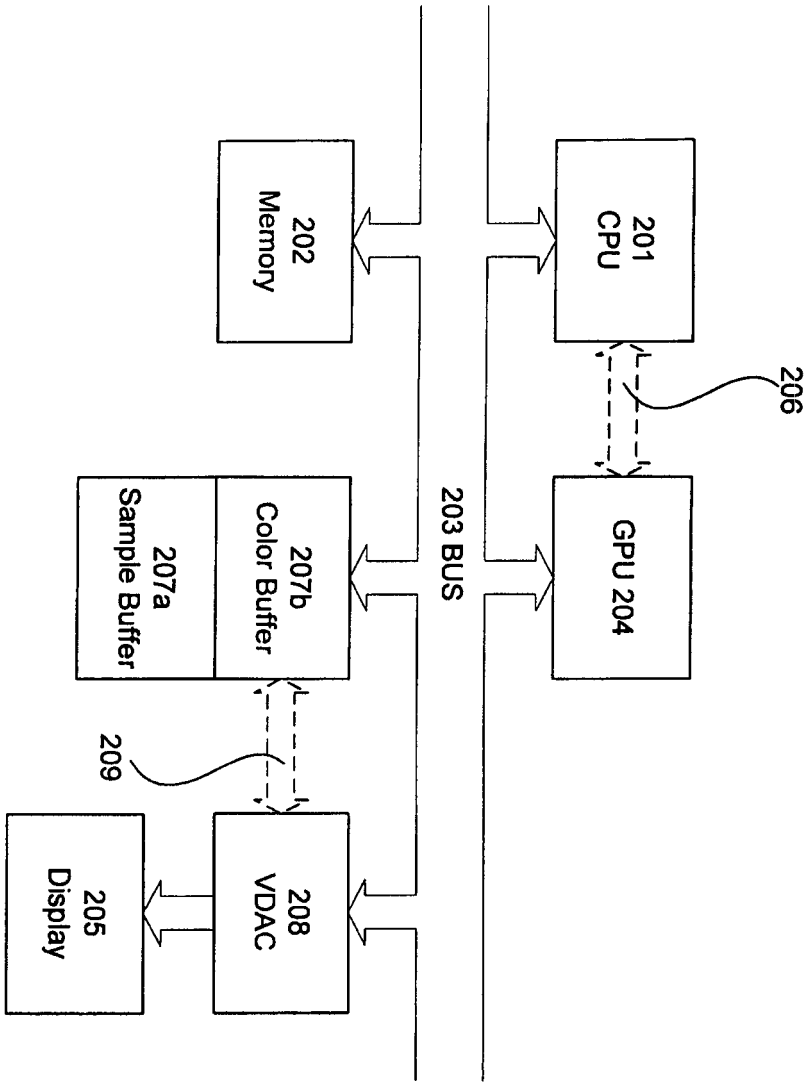
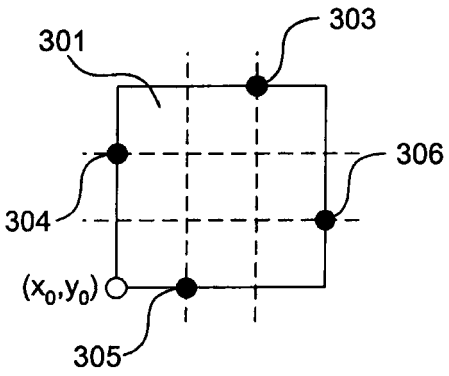

201
CPU
202
Memory
206
GPU 204
203 BUS
207b
Color Buffer
207a
Sample Buffer
209
208
VDAC
205
Display

Fig 1



Quad A

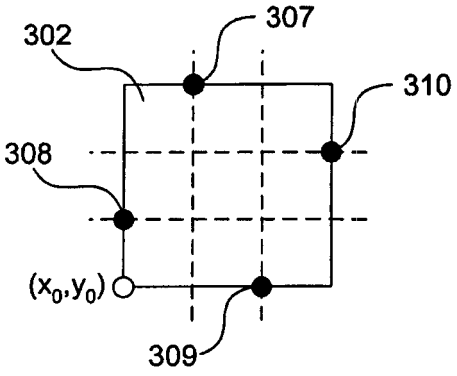
303 = (x0+2/3, y0+1)

304 = (x0, y0+2/3)

305 = (x0+1/3, y0)

306 = (x0+1, y0+1/3)

Fig 2a



Quad B

307 = (x0+1/3, y0+1)

308 = (x0, y0+1/3)

309 = (x0+2/3, y0)

310 = (x0+1, y0+2/3)

Fig 2b

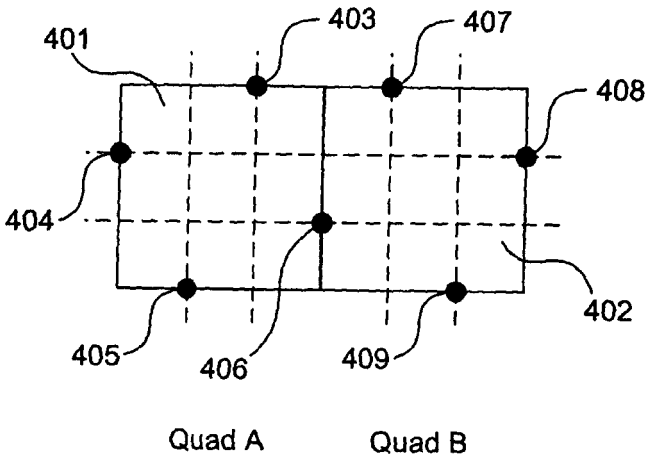
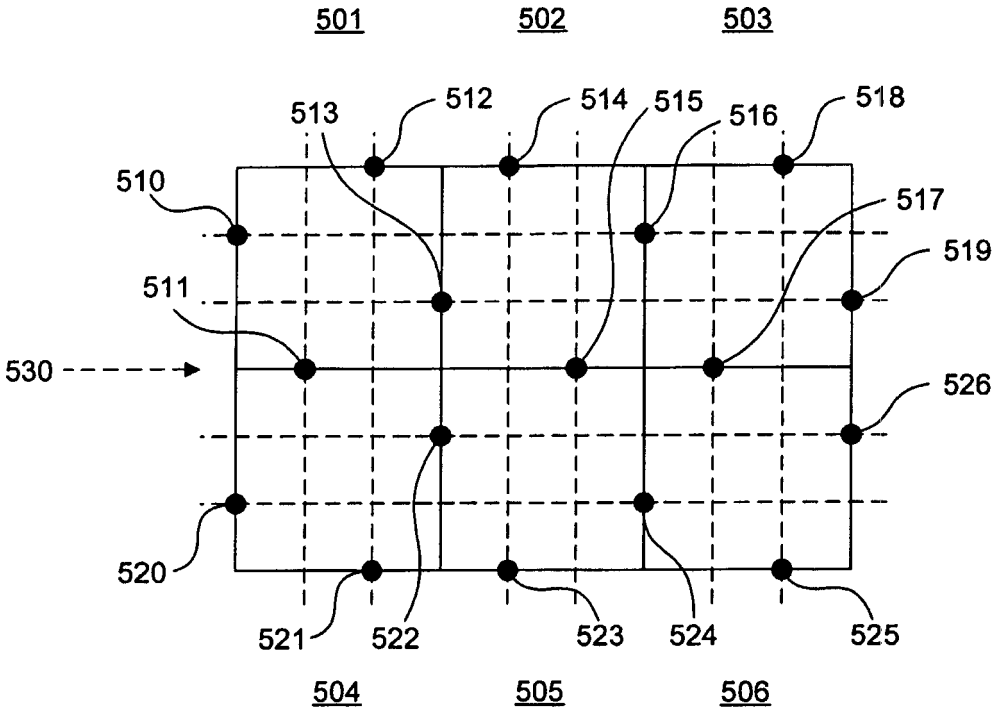


Fig 3


501
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513
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Fig 4

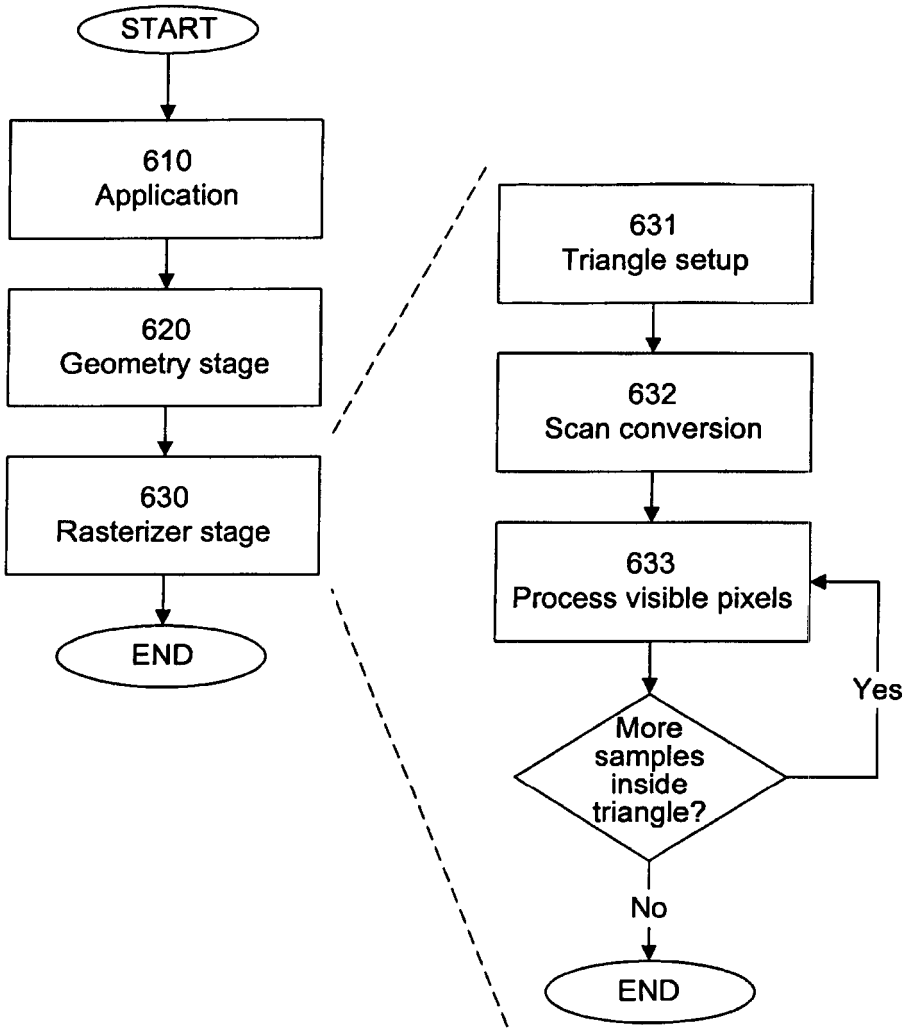
START
610
Application
620
Geometry stage
630
Rasterizer stage
END
631
Triangle setup
632
Scan conversion
633
Process visible pixels
More samples inside triangle?
Yes
No
END

Fig 5a

Fig 5b

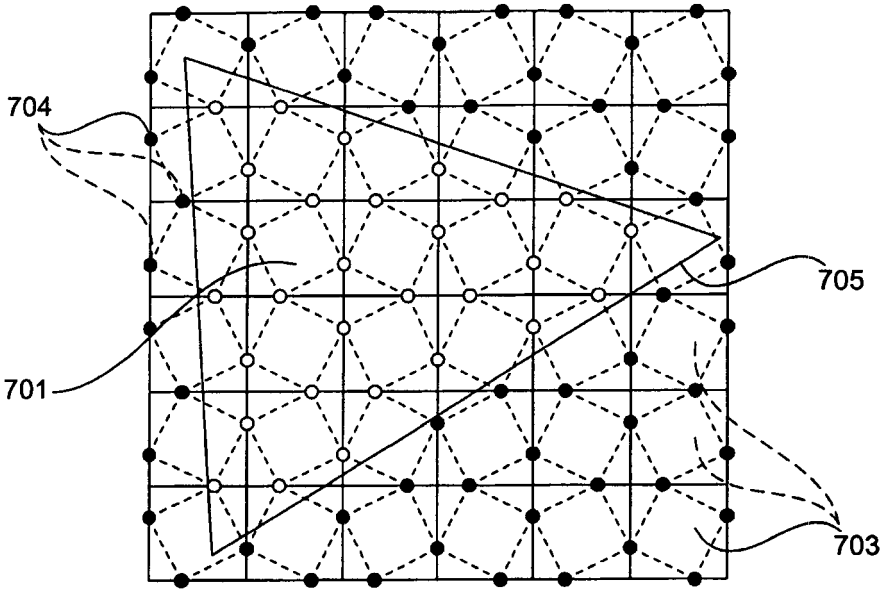

Fig 6a

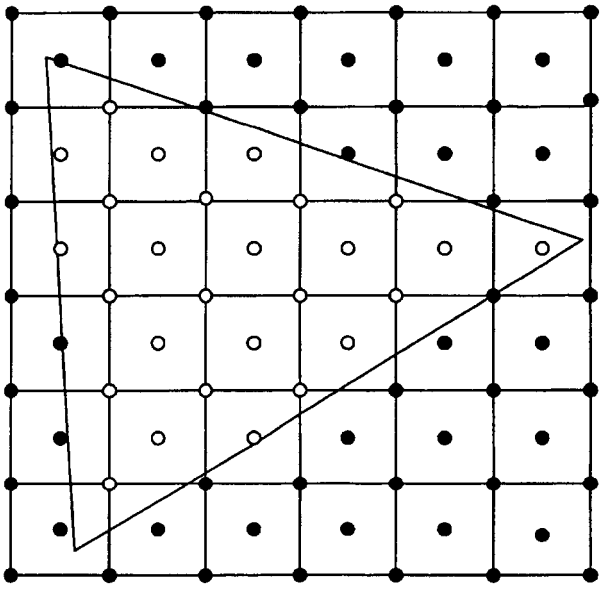

Fig 6b

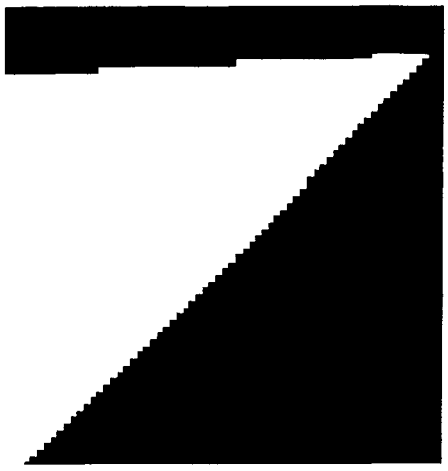

Fig 7a

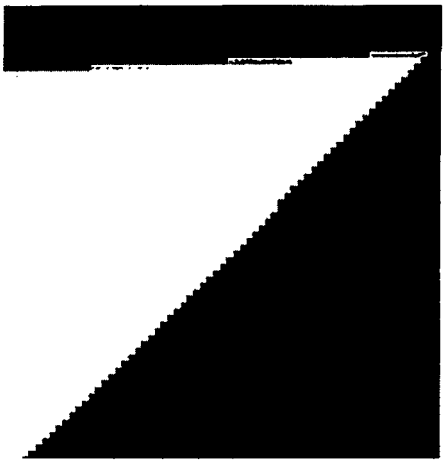

Fig 7b

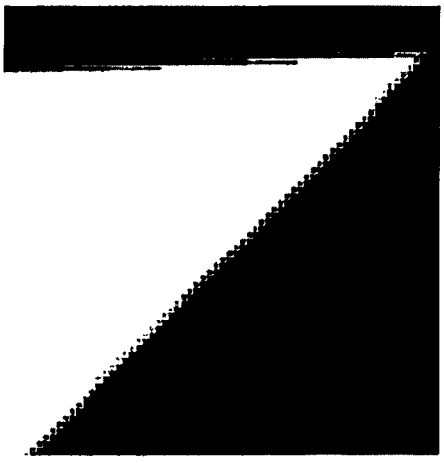

Fig 7c

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 02 8537

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A	EP 0 463 700 A (PHILIPS ELECTRONICS UK LTD ;PHILIPS NV (NL)) 2 January 1992 (1992-01-02)		

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G06T

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 July 2003	Perez Molina, E

CATEGORY OF CITED DOCUMENTS

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09-07-2003

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